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METHOD OF CLEANING SEMICONDUCTOR SURFACES

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METHOD OF CLEANING SEMICONDUCTOR SURFACES

Technical Field

This invention relates to cleaning methods. Specifically this invention relates to a method of cleaning high density semiconductor wafers, chips and assemblies of chips.

Background

The development of high density ULSI circuits with sub-micron dimensions has lead to the requirement to remove unwanted contaminants from the surface of the wafers used in the production of structures such as high density chips along with the high density multichip assemblies constructed from these chips. This becomes especially difficult in examples such as a trench in the trench capacitor; deep contacts necessitated by stacked capacitors in dynamic random access memories (DRAMS); or the use of the damascene process in the production of copper metallurgy. High density assemblies e.g. those using flip chip or cube packaging also present significant cleaning challenges. One example of a type of material to be removed includes the residuals left from a film in which all or a portion of is to be removed. One example of such a film is a photo-resist. Another example of a type of material to be removed includes incidental contaminates.

Depending upon the type of contaminant, it may be attached to the surface by mechanisms such as chemical bonding, mechanical attachment, or a combination of chemical and mechanical mechanisms. The minimum dimensions of particles to be removed has continued to decrease as the minimum feature size has decreased. This has been aggravated by the fact that the vertical dimensions in the chips have not tended to shrink as fast as the horizontal dimensions thus making relatively deeper holes for contaminate particles to be lodged in. Further, in chip assemblies, the use of smaller diameter solder balls in C4 connections have reduced the vertical dimension between the chip and the substrate thus making the removal of contaminates from the space more difficult.

What is needed is an improved method for cleaning surfaces and structures in small dimensions such those produced in semiconductor manufacture.

Summary

The above mentioned problems such as cleaning high aspect ratio features and cleaning smaller more fragile features are addressed by the present invention and will be understood by reading and studying the following specification.

A method of cleaning a semiconductor surface is provided. The method includes placing the semiconductor surface in contact with a carrier fluid. The method also includes forming a supercritical fluid adjacent to the semiconductor surface. The method then includes changing a thermodynamic condition of the supercritical fluid to cause gas bubbles in the carrier fluid. In one embodiment, the semiconductor surface includes a surface in a semiconductor assembly such as a semiconductor package or a multichip assembly.

Another method of cleaning a semiconductor surface is also provided. The method includes placing the semiconductor surface in contact with a carrier fluid. The method also includes forming a supercritical fluid adjacent to the semiconductor surface. The method then includes changing a thermodynamic condition of the supercritical fluid to cause gas bubbles in the carrier fluid. The method also includes providing supplemental mechanical energy at the semiconductor surface in addition to the gas bubbles.

A method of forming a trench capacitor is provided. The method includes forming a trench in a semiconductor surface. The method also includes cleaning the trench. Cleaning the trench includes placing the semiconductor surface in contact with a carrier fluid. Cleaning also includes forming a supercritical fluid adjacent to the semiconductor surface, and changing a thermodynamic condition of the supercritical fluid to cause gas bubbles in the carrier fluid. The method of forming a trench capacitor also includes forming an insulator layer within the trench, and forming a conductive plate over the insulator layer.

A method of forming a device contact is provided. The method includes forming an opening within an insulator layer located over a device. The method

also includes cleaning the opening. Cleaning the opening includes placing the insulator layer in contact with a carrier fluid. Cleaning the opening also includes forming a supercritical fluid adjacent to the insulator layer and changing a thermodynamic condition of the supercritical fluid to cause gas bubbles in the carrier fluid. The method of forming a device contact also includes depositing a conductor material within the opening.

Higher level devices are also provided in embodiments that include memory devices and information handling systems such as personal computers.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

FIG. 1 shows an information handling system according to an embodiment of the invention.

FIG. 2 shows a block diagram of a processing unit according to an embodiment of the invention.

FIG. 3 shows a semiconductor wafer according to an embodiment of the invention.

FIG. 4A shows a stage in processing a surface according to an embodiment of the invention.

FIG. 4B shows a stage in processing a surface according to an embodiment of the invention.

FIG. 4C shows a stage in processing a surface according to an embodiment of the invention.

FIG. 4D shows a stage in processing a surface according to an embodiment of the invention.

FIG. 5 shows a cleaning system according to an embodiment of the invention.

FIG. 6 shows a cleaning system according to an embodiment of the invention.

FIG. 7 shows selected electronic devices formed according to an embodiment of the invention.

Detailed Description

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention.

The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The term substrate is understood to include semiconductor wafers and first level packaging. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers, such as silicon-on-insulator (SOI), etc. that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term conductor is understood to include semiconductors, and the term insulator or dielectric is defined to include any material that is less electrically conductive than the materials referred to as conductors. The term chip assembly, as used in this application includes the joining of one or more chips to each other and or to a chip carrier.

The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as "on", "side" (as in "sidewall"), "higher", "lower", "over" and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

The disclosed cleaning methods and devices are particularly applicable to the cleaning of any surface with intricate or fragile features. Although a number of types of surfaces are within the scope of the invention, the cleaning of a semiconductor chip or wafer surface is used in the following description as an example. Semiconductor chips, assemblies of chips, or semiconductor wafers are included in higher level devices or methods of forming devices such as information handling systems or personal computers. In one embodiment, the personal computer shown in Figures 1 and 2 includes chips formed using methods described below.

The personal computer shown in Figures 1 and 2 includes a monitor 100, keyboard input 102 and a central processing unit 104. The processor unit typically includes microprocessor chip or chips 106, memory bus circuit 108 having a plurality of memory slots 112(a-n), and other peripheral circuitry 110. Peripheral circuitry 110 permits various peripheral devices 124 to interface processor-memory bus 120 over input/output (I/O) bus 122.

Microprocessor 106 produces control and address signals to control the exchange of data between memory bus circuit 108 and microprocessor 106 and between memory bus circuit 108 and peripheral circuitry 110. This exchange of data is accomplished over high speed memory bus 120 and over high speed I/O bus 122.

Coupled to memory bus 120 are a plurality of memory slots 112(a-n) which receive memory devices. For example, single in-line memory modules (SIMMs)

and dual in-line memory modules (DIMMs) may be used in the implementation of embodiments of the present invention. Those skilled in the art will recognize that a wide variety of memory devices with memory chips may be coupled to the plurality of memory slots 112(a-n). Acceptable memory devices include, but are not limited to, SDRAMs, SLDRAMs, RDRAMs and other DRAMs and SRAMs, VRAMs and EEPROMs, may be used in the implementation of the present invention. One of ordinary skill in the art, having the benefit of the present disclosure, will recognize that chips can be used in chip assemblies i.e. packages which include one or more chips.

Figure 3 shows a wafer 300 of semiconductor material. Semiconductor materials include, but are not limited to, silicon, gallium arsenide, silicon-on-insulator structures, etc. The wafer 300 includes a number of individual chips 310. The chips 310 may be configured to include several types of integrated circuits on single or multiple chips such as memory circuits, processor circuits, application specific circuits, etc. In one embodiment, after processing according to methods described below, the wafer 300 is divided or diced into the respective number of chips 310. The individual chips are then incorporated into higher lever systems or devices such as illustrated in Figures 1 and 2. In one embodiment, methods of cleaning a semiconductor surface are used to clean a surface of a wafer 300. In one embodiment, methods of cleaning a semiconductor surface are used to clean an individual chip 310 after a dicing operation. In one embodiment, methods of cleaning a semiconductor surface are used to clean an assembly of chips.

Figure 4A shows a portion of a semiconductor 400 including a feature 402. In one embodiment, the semiconductor 400 includes a chip or collection of chips. In one embodiment, the semiconductor 400 includes a wafer. In one embodiment, the feature 402 includes a trench. In one embodiment, the feature 402 includes a protruding feature. Other features normally used in the formation of semiconductor devices are also within the definition of the feature 402. For illustration, the feature 402 shown in Figures 4A – 4D is a trench.

A processing layer 410 is shown covering a surface 404 of the semiconductor 400. Several types of processing layers 410 are included within the

scope of the invention. In one embodiment, the processing layer 410 includes a photoresist material. In one embodiment, the processing layer 410 includes a nitride masking layer. In one embodiment, the processing layer 410 includes an oxide layer. In one embodiment, the processing layer 410 includes a metal layer. Other semiconductor fabrication layers are also within the scope of the invention. As shown in Figure 4A, the processing layer 410 is formed both on the surface 404 of the semiconductor 400 and closely contouring the feature 402.

In one embodiment, the semiconductor 400 is processed within an enclosed chamber 420. In one embodiment, the chamber 420 is used for multiple processing operations. In one embodiment, a number of separate chambers 420 are used to complete a semiconductor fabrication process. In one embodiment, a gas atmosphere 422 within the chamber can be controlled by varying a number of physical variables. In one embodiment, the variables include thermodynamic variables such as pressure, volume, and temperature.

Figure 4B shows the semiconductor 400 after a removal operation. In one embodiment, the condition of the semiconductor 400 shown in Figure 4B corresponds to a level of cleaning achieved using current cleaning methods. An unwanted particle 412 is shown remaining within the feature 402. In one embodiment the particle 412 is a fraction of material remaining from incomplete removal of the processing layer 410. In one embodiment, the particle 412 is a foreign particle that was deposited along with the processing layer 410. In one embodiment, the particle 412 includes a foreign particle from a semiconductor processing operation separate from deposition or removal of the processing layer 410.

In one embodiment, the removal operation used to create the condition in Figure 4B includes introducing a solvent solution to the surface 404 of the semiconductor 400. In one embodiment, the particle 412 remains behind after the removal operation due to incomplete dissolution of the processing layer 410 in the solvent solution. In one embodiment, the particle 412 remains behind due to a particle material that dissolves poorly or does not dissolve in the solvent solution.

Figure 4C shows the surface 404 of the semiconductor 400 and the

remaining particle 412 within the feature 402. A carrier fluid 430 is further shown adjacent to the surface 404 of the semiconductor 400. In one embodiment, the carrier fluid 430 includes the solvent solution used to remove the processing layer 410. In one embodiment, the carrier fluid 430 includes a subsequent cleaning or solvent solution. Carrier fluids include, but are not limited to, de-ionized water, H_2SO_4, and H_2O_2. In one embodiment, only selected surfaces of the semiconductor 400 are introduced to the carrier fluid 430. In one embodiment, the entire semiconductor 400 is immersed within the carrier fluid 430.

In one embodiment, the atmosphere 422 within the chamber 420 is adjusted to alter a state of the atmosphere 422. In one embodiment, the atmosphere 422 is altered during a processing time when the surface 404 of the semiconductor 400 and the feature 402 are exposed to the carrier fluid 430. In one embodiment, atmosphere is altered to change the atmosphere to a supercritical state. An atmosphere 422 or environment is determined to be in a supercritical state (and is referred to as a supercritical fluid) when it is subjected to a combination of pressure and temperature above its critical point, such that its density approaches that of a liquid (i.e., the liquid and gas states are indistinguishable). A wide variety of compounds and elements can be converted to the supercritical state.

In one embodiment, the supercritical state is achieved by varying a temperature within the chamber 420. In one embodiment, the supercritical state is achieved by varying a pressure within the chamber 420. In one embodiment, the supercritical state is achieved by varying both a temperature and a pressure within the chamber 420. In one embodiment, carbon dioxide is used to form a supercritical fluid. Carbon dioxide has advantages such as low cost, and moderate temperature and pressure conditions necessary to form a supercritical state. In a carbon dioxide embodiment, a temperature includes 32 °C and a pressure of 73 Atm.

In addition to a carbon dioxide atmosphere embodiment, other suitable atmospheres 422 include, but are not limited to, nitrous oxide, ethane, ethylene, propane, and xenon. In one embodiment, the supercritical state includes a supercritical fluid formed from one of the gases listed above. In one embodiment the supercritical fluid includes ethyl alcohol, ethyl ether or methyl alcohol.

After formation of the supercritical fluid, the supercritical fluid formed from the atmosphere 422 and the carrier fluid 430 mix together to form a substantially homogenous fluid. Under this condition, the homogenous fluid substantially surrounds the particle 412 within the feature 402.

Figure 4D shows the surface 404 of the semiconductor 400 and the remaining particle 412 within the feature 402 from Figure 4C. The atmosphere 422 within the chamber 420 is altered a second time to remove conditions within the chamber 420 from the supercritical state. Figure 4D shows a number of bubbles 424 forming at random locations within the carrier fluid 430. In one embodiment, after the supercritical conditions within the chamber 420 are removed, the supercritical fluid component of the homogenous fluid returns to a gas state, causing the bubbles 424 to form.

Figure 4D shows a bubble forming adjacent to the particle 412. The energy provided by the expanding gas of the bubble 424 dislodges the particle 412, allowing it to be flushed away by the carrier fluid. The energy provided by the expanding bubble is effective for removal of the particle 412 because it provides mechanical energy to dislodge mechanical/physical constraints on the particle 412. The energy provided by the expanding bubble is further effective to break any bonding of the particle 412 to the semiconductor 400 such as Van der Waals bonding, or electrostatic bonding.

Using a supercritical fluid as described in embodiments above has a number of advantages. Supercritical fluids are recognized as a good solvent for many types of materials. A selected supercritical fluid can therefore provide both a chemical removal mechanism for some materials, and a mechanical removal mechanism for other non-dissolved particles as described in embodiments above.

Another advantage of methods and devices described above includes a homogenous delivery of energy to the surface being cleaned. Other mechanical cleaning methods such as sonic bath cleaning can create harmonic "hot spots" at locations on the surface where constructive wave interference amplifies the mechanical energy. Although sonic bath methods add additional energy for more effective cleaning, in some cleaning situations, the sonic hot spots can damage

sensitive surface features.

Another advantage of methods and devices described above includes the ability to use supercritical fluid techniques with existing cleaning processes and cleaning solutions. For example, in a current dry cleaning process, de-ionized water is used to rinse a surface of a semiconductor surface. A supercritical fluid method as described above can be used to form bubbles in the de-ionized water. Likewise, in a wet cleaning example, a solution such as H_2SO_4 or H_2O_2 is used to clean the semiconductor surface. A supercritical fluid method as described above can be added to this wet cleaning example to form bubbles in the H_2SO_4 or H_2O_2 solutions. In processes such as those used for multichip assemblies where fluxes and or organic residues are present, chlorocarbons or chlorofluorocarbons may be used as a carrier fluid.

Figure 5 shows a cleaning system 500. A portion of a semiconductor 510 is shown including a feature 512. An unwanted particle 514 is shown within the feature. A carrier fluid 520, similar to carrier fluids described in embodiments above, is shown in contact with a surface 504 of the semiconductor 510. Similar to embodiments described above, the surface 504 of the semiconductor, the feature 512 and the particle 514 are contained within a chamber 540. The atmosphere 542 within the chamber 540 can be controlled to produce a supercritical state. As described in embodiments above, mechanical energy for cleaning particles such as particle 514 is provided by altering a supercritical state to produce bubbles.

In addition to the use of the supercritical state for mechanical energy, a sonic wave generation system 530 is shown in block diagram form, coupled to the carrier fluid 520. In some embodiments, mechanical energy in addition to that provided by the supercritical fluid is desirable for removal of unwanted particles. In one embodiment, the sonic wave generation system 530 includes ultrasonic energy. In one embodiment, the sonic wave generation system 530 includes megasonic energy. Other frequencies of wave generation are also within the scope of the invention.

Figure 6 shows a cleaning system 600. A portion of a semiconductor 610 is shown including a feature 612. An unwanted particle 614 is shown within the feature. A carrier fluid 620, similar to carrier fluids described in embodiments

above, is shown in contact with a surface 604 of the semiconductor 610. Similar to embodiments described above, the surface 604 of the semiconductor, the feature 612 and the particle 614 are contained within a chamber 640. The atmosphere 642 within the chamber 640 can be controlled to produce a supercritical state. As described in embodiments above, mechanical energy for cleaning particles such as particle 614 is provided by altering a supercritical state to produce bubbles.

In addition to the use of the supercritical state for mechanical energy, a brush cleaning system 630 with a number of bristles 632 is shown in block diagram form, in contact with the surface 604. In some embodiments, the mechanical energy supplied by the brush cleaning system 630 is desirable for removal of unwanted particles in addition to the energy provided by the supercritical fluid as described in embodiments above.

Figure 7 shows examples of devices that are fabricated using semiconductor processing techniques. Devices formed using cleaning methods described below include, but are not limited to, trench capacitors and device contacts, etc. Devices shown in Figure 7 are not necessarily drawn to scale. Further, the devices shown in Figure 7 are shown isolated from other components, connecting structures, and devices for the purpose of illustration.

A portion of a chip 700 is shown, including a trench capacitor 710 formed in a semiconductor substrate 702. The trench capacitor 710 includes an insulator layer 712 and a plate 714 within the insulator layer 712. In one embodiment, the substrate functions as a second plate of the trench capacitor 710. An aspect ratio of the trench capacitor 710 is shown as the depth 716 divided by the width 718. As shown in Figure 7, the trench capacitor 710 includes a high aspect ratio design, that requires a deep and narrow trench.

Advantages such as the homogenous supply of energy from a supercritical fluid enables more effective cleaning of high aspect ratio features such as the trench of a trench capacitor 710. While a brush may not penetrate to depths of features such as the trench of a trench capacitor 710, using embodiments as described above, bubbles will form deep within the trench to provide mechanical energy for unwanted particle removal.

A transistor 720 is shown located on the semiconductor substrate 702. The transistor includes a first source/drain region 722, a second source/drain region 724, and a channel region 726 between the first source/drain region 722 and the second source/drain region 724. A dielectric layer 728 is located over the channel region 726, and a gate 730 is located over the dielectric layer 728. Although a lateral transistor configuration is shown as an example, other transistor configurations such as a vertical transistor are also within the scope of the invention. An isolation layer 704 is shown located over and around the transistor 720. Layers such as the isolation layer 704 are used in some integrated circuits to electrically isolate the transistor 720 and to space apart additional layers of devices and interconnection structures (not shown).

When additional layers such as the isolation layer 704 are formed over a transistor 720, electrical connections must be made through the isolation layer 704 to operate the transistor 720. A first opening 732 is shown over the first source/drain region 722, and a second opening 734 is shown over the second source/drain region 724. The thickness 740 of the isolation layer 704 and a width 742 of the openings 732, 734 determines an aspect ratio of the contact openings. Although a conductor structure or device is eventually deposited within the first opening 732 and the second opening 734, it is frequently necessary to clean the opening 732 and the second opening 734 during fabrication.

Similar to the trench capacitor example described above, advantages such as the homogenous supply of energy from a supercritical fluid enables more effective cleaning of high aspect ratio features such the first opening 732 and the second opening 734. While a brush, or sonic energy may not penetrate to depths of features such as the first opening 732 and the second opening 734, using embodiments as described above, bubbles will form deep within the openings to provide mechanical energy for unwanted particle removal.

In one application, after the wafer processing is complete, chips are diced and joined into higher level assemblies. Prior to joining it may be desirable to clean the chips to remove debris from the dicing apparatus. Likewise in one embodiment,

after assembly, the narrow spaces between chips and or between chips and the substrate are cleaned to remove unwanted residue from the joining/assembly processing.

Although devices such as a trench capacitor 710 and a transistor 720 are shown as examples of devices that benefit from the cleaning methods described above, the invention is not so limited. Other electronic devices and features are within the scope of the invention.

Conclusion

Devices and methods of cleaning described in embodiments above have a number of advantages. Advantages of cleaning using a supercritical fluid include a combination of both chemical and mechanical removal abilities from the supercritical fluid. The mechanical energy in embodiments described above is transmitted in an improved homogenous manner throughout a carrier fluid. The mechanical energy in embodiments described above is also improved in an ability to use with delicate surface features. Supercritical fluid methods as described in embodiments above are also easily integrated into existing cleaning methods.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention includes any other applications in which the above structures and fabrication methods are used. The scope of the invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.